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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,434	09/23/2003	Pinghai Hao	TI-35470	2415
23494	7590	05/03/2005		EXAMINER NGUYEN, KHIEM D
				ART UNIT 2823
				PAPER NUMBER

DATE MAILED: 05/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/670,434	HAO ET AL.	
	Examiner	Art Unit	
	Khiem D. Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 14 February 2005.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-27 is/are pending in the application.
 4a) Of the above claim(s) 23-27 is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-22 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 23 September 2003 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date: _____
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>09/23/03</u> .	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Group I, claims 1-22 in the reply filed on February 14th, 2005 is acknowledged.

Oath/Declaration

The oath/declaration filed on September 23rd, 2003 is acceptable.

Information Disclosure Statement

The Information Disclosure Statement filed on September 23rd, 2003 has been considered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 5, 8-14, and 17-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Mandelman et al. (U.S. Pub. 2003/0020125).

In re claim 1, Mandelman discloses a method for fabricating a transistor structure, comprising: implanting a first dopant 71 that penetrates into a lightly doped drain (LDD) region 90, 95 to a depth less than a LDD junction depth (page 4, paragraphs [0050]-[0052] and FIGS. 7-8a); and

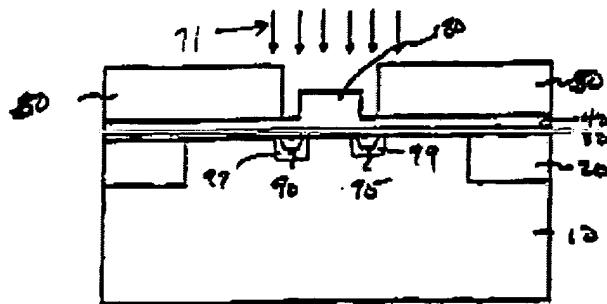


Figure 7

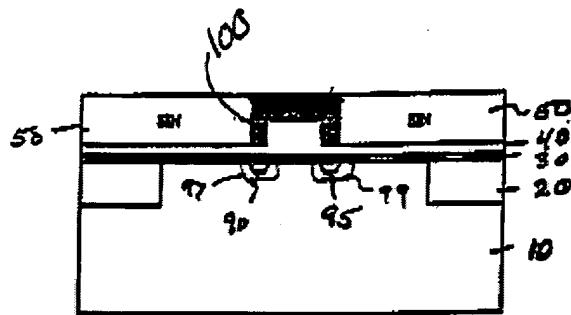


Fig. 8a

implanting a second dopant beyond the LDD junction depth to form a source/drain region 130, the implantation of the second dopant overpowering a substantial portion of the first dopant to define a floating region 97, 99 of the first dopant within the LDD region 90, 95 (page 4, paragraph [0057] and FIGS. 9-10).

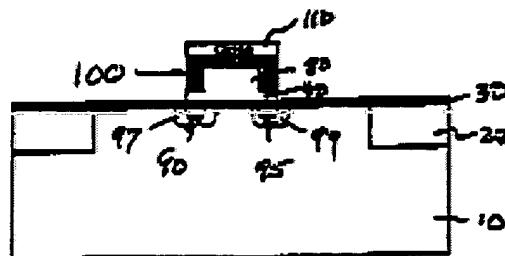


Fig. 9

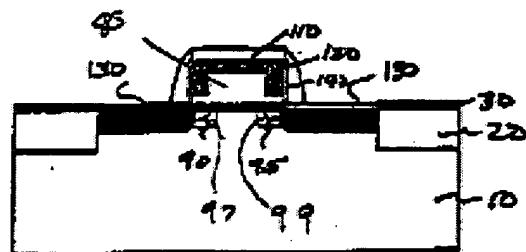


Fig. 10

In re claim 2, Mandelman discloses that the floating region further comprising a floating ring 97, 99 substantially self-aligned with an edge of a gate 40, 80 of the transistor structure (page 4, paragraph [0057] and FIGS. 9-10).

In re claim 3, Mandelman discloses that the method of claim 1, further comprising forming the LDD region 90, 95 by implanting a dose of a third dopant that is greater than a dose of the first dopant (page 4, paragraphs [0050]-[0052] and FIGS. 9-10).

In re claim 5, Mandelman discloses that the at least one of the implantation of the first dopant 71 and the implantation of the third dopant employing tilted angle implants to enhance an amount of overlap between a gate structure of the transistor structure and the LDD region (FIGS. 9-10).

In re claim 8, Mandelman discloses that the transistor structure is a complimentary metal oxide semiconductor (CMOS) structure that includes a gate **40, 80** having a side edge portion, the floating region **97, 99** being substantially aligned with the side edge portion of the gate **40, 80** (page 4, paragraph [0057] and FIGS. 9-10).

In re claim 9, Mandelman discloses that the CMOS structure is an n-channel CMOS structure, the first dopant **71** forming a shallow region in the LDD region that comprises a p-type dopant (page 4, paragraph [0050] and FIG. 7).

In re claim 10, Mandelman discloses that the first dopant **71** comprises boron, and the floating region **97, 99** further comprises a boron floating ring, substantially aligned with side edge portion of the gate **40, 80** (page 4, paragraph [0057] and FIGS. 9-10).

In re claim 11, Mandelman that the CMOS structure is a p-channel CMOS structure, the first dopant **71** defining a shallow region that comprises an n-type dopant (page 4, paragraph [0050] and FIG. 7).

In re claim 12, Mandelman discloses that the method of claim 1, further comprising: forming a gate structure **40, 80** above the substrate **10**, the LDD region **90, 95** and the source/drain region **130** being formed in the substrate **10** generally around the gate structure **40, 80**, the gate structure overlapping at least a substantial portion of the LDD region **90, 95** and the floating ring **97, 99** being substantially aligned with an edge of the gate structure **40, 80** (page 4, paragraph [0057] and FIGS. 9-10).

In re claim 13, Mandelman discloses a method for fabricating a CMOS transistor device, comprising forming a gate structure **40, 80** on a substrate **10**, the gate structure **40, 80** having a side edge (page 4, paragraph [0050] and FIGS. 7 and 8a);

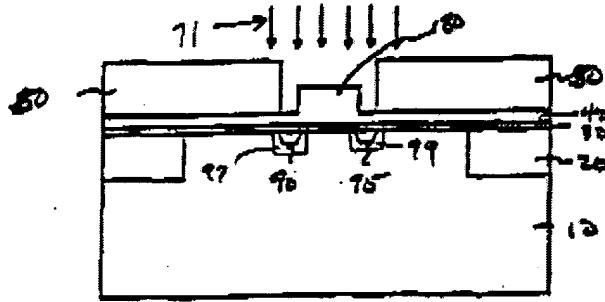


Figure 7

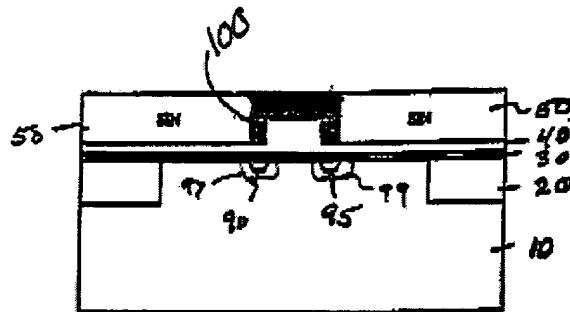


Fig. 8a

forming a lightly doped drain (LDD) region **90, 95** in the substrate **10** laterally of a channel region (page 4, paragraphs [0050]-[0052] and FIG. 7);
forming a shallow region in the LDD region **90, 95** that extends into the substrate **10** to a depth that is less than an LDD junction depth (page 4, paragraph [0050]); and forming a source/drain region **130** substantially, the formation of the source/drain region resulting in forming a floating structure **97, 99** from the shallow region that is

located in the LDD region and generally aligned with the side edge of the gate structure **40, 80** (page 4, paragraph [0057] and FIGS. 9-10).

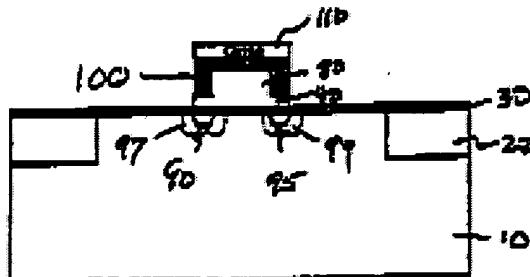


Fig. 9

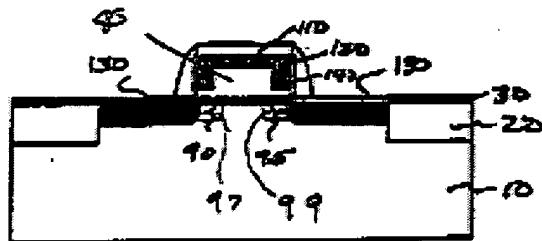


Fig. 10

In re claim 14, Mandelman discloses that the LDD region **90, 95** being formed with a dose of a dopant that is greater than a dose of a dopant utilized to form the shallow region (page 4, paragraph [0050] and FIG. 7).

In re claim 17, Mandelman discloses that the at least one of the implantation of the formation of the LDD region **90, 95** and the formation of the shallow region further comprising employing tilted angle implants to increase an amount of overlap beneath the gate structure **40, 80** (FIGS. 9-10).

In re claim 18, Mandelman discloses that the formation of the source/drain region 130 being implemented with a dose of a dopant that is greater than a dose of a

dopant utilized to form each of the LDD region **90, 95** and the shallow region (page 4, paragraph [0057] and FIGS. 9-10).

In re claim 19, Mandelman discloses that the CMOS structure is an n-channel CMOS structure, the shallow region comprising a p-type dopant (page 4, paragraph [0050] and FIG. 7).

In re claim 20, Mandelman discloses that the shallow region comprising boron, the floating structure comprising a boron floating ring **97, 99** substantially aligned with the side edge of the gate structure **40, 80** (page 4, paragraph [0057] and FIGS. 7-10).

In re claim 21, Mandelman discloses that the CMOS structure is a p-channel CMOS structure, the shallow region comprising an n-type dopant (page 4, paragraph [0050] and FIG. 7).

In re claim 22, Mandelman discloses that a transistor structure formed according to the method of claim 13 (page 4, paragraphs [0050]-[0057] and FIGS. 7-10).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 4, 6, 7, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mandelman et al. (U.S. Pub. 2003/0020125).

In re claims 4, 6, 7, 15, and 16, Mandelman discloses that the heavier source/drain implants 97, 99 would be made after the formation of the sidewall spacers 140 (page 4, paragraph [0057] and FIGS. 9-10)

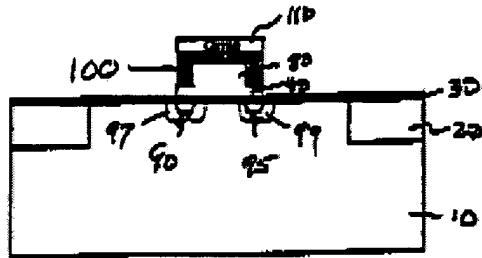


Fig. 9

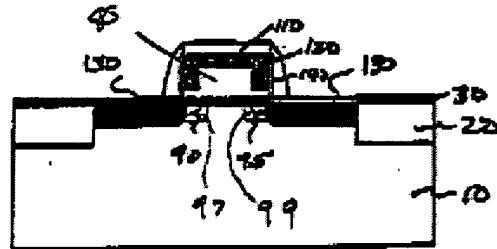


Fig. 10

but does not explicitly disclose the dopant ranges of the first, second, and third dopants. However, there is no evidence indicating the dopant ranges of the first, second and third dopants is critical and it has been held that it is not inventive to discover the optimum or workable range of a result-effective variable within given prior art conditions by routine experimentation. See MPEP § 2144.05. Note that the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising there from. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the

chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D. Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:30 AM - 5:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



K.N.
April 29th, 2005

W. DAVID COLEMAN
PRIMARY EXAMINER